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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/047,320	LI, RAYMOND	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-24* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The response filed on 8/13/2008 has been fully considered in preparing for this Office Action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene (U.S. Patent No. 5,553,220) in view of Dutton (U.S. Patent No. 5,802,330).

As per claim 1, as shown in Fig. 2, Keene teaches *a video graphics and audio processing circuit comprising:*

a graphics processing circuit (209)*;*

an audio processing circuit (201)*;*

a local bus (internal bus inside the multimedia adapter 202) *operative to receive incoming data from a system bus* (109) *and operatively coupled to transceive data to and from the graphics processing circuit and the audio processing circuit; and*

a bus arbitrator operatively coupled to the local bus, the graphics processing circuit, and the audio processing circuit (host CPU interface 210 and the memory controller/arbitrator 211)*, wherein the bus arbitrator interprets the incoming data and provides the incoming data to the audio processing circuit or to the video graphics processing circuit* (col. 3, lines 62-65)*,*

Keene fails to explicitly teach *the bus arbitrator arbitrates outputting data on the local bus from the graphics processing circuit and the audio processing circuit.* However, this is what Dutton teaches. As shown in Fig. 1, Dutton teaches a computer system, comprising a graphics processor 170, audio processor 172, and a system bus (CPU bus 104), local bus 120, and a bus arbiter 180 to arbitrate the ownership of different devices including the graphics processor and the audio processor on the local bus 120 (col. 4, lines 18-36).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Keene in order to allow real time devices to obtain adequate access to the system busses and the bus arbitration is dynamically varied to account for varying requirements of the system (col. 2, lines 14-17).

As per claim 2, Keen teaches *the bus arbitrator comprises an address decoder operatively coupled to receive an address via the local bus, to route received data to the audio processing circuit when the address identifies the audio processing circuit and to route received data to the graphics processing circuit when the address identifies the graphics processing circuit* (see col. 9, lines 16-40).

As per claim 3, Keene further teaches the address decoder comprises control circuitry that generates an output data control signal based on the address and a data command signal (in order to forward to the graphics or audio processors, see also col. 3, lines 62-65).

As per claim 4, Keene further teach the bus arbitrator further comprises an output data switch operatively coupled to output data to the bus from the audio processing circuit or the graphics processing circuit based on the output data control signal (such as the memory

controller / arbitrator 211 to switch the output from the audio and graphics processors to memory 101).

As per claim 6, as cited above, Keene teaches *a method for bus arbitration between an audio processing circuit and a graphics processing circuit, the method comprises*

a) receiving at least one address;

b) determining whether the at least one address identifies at least one of: the audio processing circuit and the graphics processing circuit (this is done by the single host CPU interface 210 as cited above) *; and*

c) when the at least one address identifies both the audio processing circuit and the graphics processing circuit (since Keene teaches the audio data buffer is allocated in the same graphics memory (Fig. 2), and the size and location of the audio buffer is dynamically allocated in the same memory, and further teaches the timing of audio data transfer into and out of the display memory is controlled by a video horizontal sync signal, it is implied that there's a chance a location in the display memory identifies both audio processing circuit and graphics processing circuit, see col. 3, lines 50-65)

Keen fails to teach *arbitrating access to a local bus between the audio processing circuit and the graphics processing circuit.* However, as cited above referring to claim 1, Dutton teaches this feature.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Keene in order to allow real time devices to obtain adequate access to the system busses and the bus arbitration is dynamically varied to account for varying requirements of the system (col. 2, lines 14-17).

As per claim 7, as shown in Fig. 2, since the data provided from the CPU includes data, address and controls, it is implied that (a) further comprises receiving an associated command for each of the at least one address.

As per claims 8 and 10, as cited above and shown in Figs. 2-3, Keene further teaches enabling the audio processing circuit to receive incoming data via the local bus when at least one address identifies the audio processing circuit (as cited above) and when the associated command is for inputting/outputting data (i.e. write/read data).

As per claims 9 and 11, as cited above, Keene teaches enabling the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting/outputting data (i.e. write/read data).

As per claim 12, it is inherent that the at least one address comprises a plurality of addresses.

As per claim 13, although not taught by Keene, Dutton teaches intermixing the audio processing circuit's access to the local bus with the graphics processing circuit's access to the local bus based on the plurality of addresses and the associated command (depending on the priority level of the request device).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Keene in order to allow real time devices to obtain adequate access to the system busses and the bus arbitration is dynamically varied to account for varying requirements of the system (col. 2, lines 14-17).

Claims 14 and 17, which are similar in scope to claim 6, are thus rejected under the same rationale.

As per claim 15, as cited above, Keene teaches the memory further comprises programming instructions that cause the processing unit to determine whether the associated data command is for inputting data or outputting data (i.e. command to write or read data).

Claim 16, which is similar in scope to claim 13, is thus, rejected under the same rationale.

Claims 18-23, which are similar in scope to claims 7-11, and 13, are thus rejected under the same rationale.

As per claim 24, although the combined Keene-Dutton does not explicitly teach the graphics processing unit, the audio processing unit, and the bus arbitrator are configured on a single chip, it would have been obvious to one skilled in the art to integrate all these components into a single chip since by doing so, the circuit can be more compact, and less bus wiring.

Allowable Subject Matter

3. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art taken singly or in combination does not teach or suggest, a video graphics and audio processing circuit, among other things, comprising a multiplexor operatively coupled to the audio buffer and the graphics buffer, wherein the multiplexor outputs the audio output data or the graphics output data based in the output data control signal.

Response to Arguments

Applicant's arguments filed 8/13/2008 have been fully considered but they are not persuasive. In response to Applicant's argument that the cited reference fails to teach a bus arbitrator operatively coupled to the local bus, the graphics processing circuit, and the audio processing circuit, wherein the bus arbitrator interprets the incoming data and provides the incoming data to the audio processing circuit or to the video graphics processing circuit, and wherein the bus arbitrator arbitrates outputting data on the local bus from the graphics processing circuit and the audio processing circuit, the examiner disagrees. As disclosed in column 3, lines 62-65, Keene teaches *the single, unified host CPU interface and related circuitry is preferably used for control or data transfer functions related to both video graphics and audio*. Thus, the host CPU interface 210 receives, interprets, and provides video graphics data and audio data to the corresponding graphics processing circuit 209 and audio processing unit 208 respectively (see Fig. 2). Also, since the host CPU interface receives and provides audio data from the host CPU bus 109 (see Fig. 3, and col. 5, line 66 to col. 6, line 17), and since the video graphics data and audio data are processed in a timely manner (i.e., audio data is processed during the "pauses", see Fig. 6, and col. 8, line 39 to col. 9, line 2), the host CPU interface 210 should be able to recognize and provide audio data and graphics data to the respective processing circuits, otherwise access conflicts between video data and audio data will be encountered (col. 9, lines 1-2). For at least this reason, the host CPU interface is considered a single local bus. Dutton teaches *the bus arbitrator to arbitrate output data on the local bus from the graphics processing circuit and the audio processing circuit* as cited above (see Dutton, col. 4, lines 18-36).

Therefore, it would have been obvious to one skilled in the art to utilize the combined teachings of Keene and Dutton to obtain the advantage mentioned in the rejection.

The examiner also disagrees with Applicant's argument that the cited reference fails to teach *when the at least one address identifies both the audio processing circuit and the graphics processing circuit* because Keene teaches the audio address and video address is similar in the host address space (e.g., start address, see col., lines 40-47). Therefore, the host CPU interface inherently identifies which data it provides to the corresponding processing circuit.

As per claims 14 and 17, Keene teaches the multimedia adapter 202 is interpreted as the single processing circuit that processes audio and video data as claimed, and also teaches a memory 101 coupled to the processing circuit 202 (see Fig. 2). Since the CPU reads and writes audio and video data into this same memory using similar host address space as cited above, identification of the associated address to the audio processing and video processing is inherently included to avoid access conflicts mentioned above. Dutton's teachings is utilized to disclose the arbitration on the local bus between the audio processing circuit and the video processing circuit as also cited above.

For at least the above reasons, the cited reference meets the minimum requirements of the claims, rejection is maintained.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628